REMARKS

Reconsideration of the application in view of the above amendments and the following remarks is requested. Claims 15, 19 and 38-56 are in this application. Claims 15 and 45 have been amended. Claims 51-56 have been added to additionally and alternately claim the present invention.

The Examiner rejected claims 15, 19, 38-39, and 45-50 under 35 U.S.C. §112, first paragraph. Specifically, the Examiner argued that FIG. 16 depicts a plurality of positive lines that are connected to pads via ESD switches, and claim 15 recites a plurality of second diodes that are connected to a pad and a positive line. The Examiner also argued that there is no support for a plurality of positive lines that are not connected to pads, as recited in claim 15.

Claim 15 recites, in part,

> "a plurality of ESD positive lines, the plurality of positive lines not being electrically connected to each other, none of the positive lines being connected to a pad."

With reference to applicant's FIG. 16, ESD positive wires 1640-1647 can be read, for example, to be the plurality of ESD positive lines. As described in applicant's specification (see page 34, lines 9-15), and as shown in applicant's FIG. 16, ESD positive wires 1640-1647 are electrically isolated from each other. As further shown in applicant's FIG. 16, none of the positive wires 1640-1647 are connected to a pad. As a result, claims 15, 19, 38 -39, and 45-50 are believed to satisfy the requirements of the first paragraph of section 112.

The Examiner rejected claims 15, 19, 38-39, and 40-45 under 35 U.S.C. §103(a) as being unpatentable over Gens et al. (U.S. Patent No. 6,055,268) in view of the Admitted Prior Art (APA). For the reasons set forth below, applicant respectfully traverses this rejection.

Claim 15 recites, in part,

> "a plurality of pads; [and]
> "a plurality of ESD positive lines, the plurality of positive lines not being electrically connected to each other, none of the positive lines being connected to a pad. [Brackets added.]

In rejecting the claims, the Examiner pointed to pads P1 and P2 shown in FIG. 2 of Gens as constituting the plurality of pads, and the horizontal lines connected to the right side of the high-power supply terminals labeled VDD1 and VDD2 as being the plurality of positive lines in Gen's structure.

However, the horizontal lines connected to the right side of the high-power supply terminals labeled VDD1 and VDD2 can not be read to be the plurality of positive lines required by claim 15 because VDD1 and VDD2 are pads.

Gens teaches, at column 3, lines 37-38,

> "The integrated circuit also includes conventional input/output pads P1, P2, . . ."

Gens also teaches, at column 3, lines 43-47,

> "In addition, according to the invention, each of the high and low power supply pads, VDD1 and VDD2, . . . VSS1 and VSS2, . . ., respectively, is also connected to buses R1 and R2 through forward and reverse biased diodes D1 and D2, respectively."

Thus, the Gens reference expressly teaches that the boxes P1, P2, VDD1, VDD2, VSS1, and VSS2 are pads. Boxes P1 and P2 are I/O pads, boxes VDD1 and VDD2 are power supply pads, and boxes VSS1 and VSS2 are ground pads.

The third amended claim 15 required that the positive lines not be connected to the pads. However, the lines identified by the Examiner as being the positive lines of claim 15 are connected to pads VDD1, VDD2, VSS1, and VSS2. Thus, the Examiner appears to be arguing (applicant apologizes for any mischaracterization of the Examiner's argument) that

I/O pads P1 and P2 can to be read pads, power supply and ground pads VDD1, VDD2, VSS1, and VSS2 can be read to be something other than pads, and therefore the lines connected to pads VDD1, VDD2, VSS1, and VSS2 are not connected to pads.

The Examiner has not cited, nor is applicant aware, of any authority that holds that when a reference teaches the presence of an element, in this case a pad, that the element can be ignored by simply reading to element to be something other than what the reference expressly teaches the element to be. However, solely for the purpose of furthering prosecution, applicant has amended claim 15 to recite, in part, "none of the positive lines being connected to a pad."

As a result, even if the phrase "a plurality of pads" required by claim 15 can be read to be only I/O pads P1 and P2, the phrase "connected to a pad" is not so limited, and can be read to be any pad, including power supply and grounds pads P1, P2, VDD1, VDD2, VSS1, and VSS2. Thus, the horizontal lines connected to the right side of power supply and ground pads VDD1 and VDD2 of Gens can not be read the plurality of positive lines required by claim 15.

As there appear to be no other structures which can be read to be the plurality of positive lines, claim15 is patentable over the Gens reference in view of the APA. In addition, since claims 19, 38-39, and 45-50 either directly or indirectly depend from claim 15, claims 19, 38-39, and 45-50 are patentable over the Gens reference in view of the APA for the same reasons as claim 15.

(As a note of correction, the Examiner summarized applicant's position in item 8 of page 6 as arguing that "the plurality of lines must be connected to the pads." Applicant argued the opposite position, stating that "the plurality of positive lines must not be connected to the pads." See page 5, lines 8-9 of applicant's January 16, 2002 Amendment.)

With further respect to claim 45, this claim has been amended to recite, in part,

"wherein the ESD positive lines are never connected to a steady voltage source."

In rejecting the claims, the Examiner pointed to column 3, lines 32-49 of Gens as teaching that the ESD protection circuit operates with a plurality of off power supplies. However, the lines connected to power supply pads VDD1 and VDD2 are connected to a steady voltage source when power is applied. As a result, Gens fails to teach or suggest that the ESD lines are never connected to a steady voltage source. As a result, claim 45 is patentable over Gens in view of the APA for this additional reason as well.

With respect to the restriction of claims 40-44, applicant agrees that two independent claims can be restricted for being related as combination and subcombination. This, however, does not apply to independent and dependent claims because a dependent claim can never be directed to an invention that is different from the independent claim. The purpose of restriction practice is to prevent a patent from issuing that claims more than one invention. If only one independent claim is present, then it is impossible to claim more than one invention. Applicant wishes to petition for review of the Examiner's decision to withdraw claims 40-44 and, as a result, respectfully requests that the Examiner reinstate claims 40-44, or declare the restriction final.

With respect to new claim 51, this claim recites, in part,

> "a plurality of ESD switches connected to the ESD positive lines and the ESD negative ring so that each positive line is connected to the negative ring via an ESD switch, a switch of the plurality of ESD switches passing a current from a positive line to the negative ring when a voltage on the positive line rises at a predetermined rate."

Applicant respectfully remains unclear as to which structures the Examiner is reading to be the plurality of ESD switches. If the Examiner is reading the horizontal lines connected to the right side of the pads VDD1 and VDD2 as being the plurality of positive lines in FIG. 2 of Gens, then the Examiner must be reading the diode D2 that is connected to pad VDD1 as being a switch. Applicant notes, however, that a current does not flow from a horizontal line that is connected to pad VDD1 to the negative ring R2 through the diode D2 that is connected to pad VDD1. As a result, the diode D2 connected to pad VDD1 can not be read to be a switch.

The ESD circuit shown in FIG. 2 of Gens provides a low resistance current path between two pads when an ESD event occurs, such as an ungrounded person handling the device. When, for example, a large positive voltage differential occurs across pads P1 and VDD1, pad P1, having the higher voltage, forward biases the diode D1 that is connected to pad P1.

When diode D1 becomes forward biased, current flows onto bus R1, thereby causing the voltage on bus R1 to rise. The increased voltage breaks the down zener diode Z which, in turn, causes current to flow onto bus R2, thereby causing the voltage on bus R2 to rise. This forward biases the diode D2 that is connected to pad VDD1, thereby causing current to flow through diode D2 to pad VDD1. As a result, a current does not flow from a horizontal line (a positive line) to bus R2 (the negative ring) through the diode D2 that is connected to pad VDD1 as required by new claim 51. As a result, the diode D2 connected to pad VDD1 can not be read to be a switch.

Thus, since a current can not flow from the positive line to the negative ring as required by new claim 51, new claim 51 is patentable over Gens et al. in view of the APA. In addition, since new claims 52-56 depend either directly or indirectly from new claim 51, claims 52-56 are patentable over Gens et al. in view of the APA for the same reasons as claim 51.

Thus, for the foregoing reasons, it is submitted that all of the claims are in a condition for allowance. Therefore, the Examiner's early re-examination and reconsideration are respectively requested.

Respectfully submitted,

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Dated: 5-7-02 By: _____

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APPENDIX

In the Claims

Please amend the claims as follows:

15. (Fourth Amendment) A semiconductor chip having a substrate of a first conductivity type, the chip comprising:

a plurality of pads;

an electrostatic discharge (ESD) negative ring:

a plurality of ESD positive lines, the plurality of positive lines not being electrically connected to each other, [the plurality of] none of the positive lines [not] being connected to [the pads] a pad;

a plurality of ESD switches connected to the ESD positive lines and the ESD negative ring so that each positive line is connected to the negative ring via an ESD switch;

a plurality of first diodes connected to the pads so that each first diode is connected to a pad and the negative ring; and

a plurality of second diodes connected to the pads so that each second diode is connected to a pad and a positive line.

45. (Amended) The chip of claim 15 wherein the ESD positive lines are [not] never connected to a steady voltage source."

Claims 51-56 have been added.